REMARKS

Reconsideration of this application is respectfully requested in light of the foregoing amendments and the following remarks.

Claims 1, 2, and 3 have been amended for reasons unrelated to patentability, including at least one of: to explicitly present one or more elements implicit in the claim as originally written when viewed in light of the specification thereby not narrowing the scope of the claim, to detect infringement more easily, to enlarge the scope of infringement, to cover different kinds of infringement (direct, indirect, contributory, induced, and/or importation, etc.), to expedite the issuance of a claim of particular current licensing interest, to target the claim to a party currently interested in licensing certain embodiments, to enlarge the royalty base of the claim, to cover a particular product or person in the marketplace, and/or to target the claim to a particular industry.

Claims 1-3 are now pending in this application. Claims 1-3 are the independent claims.

I. The Objection to Claims 1 and 3

Claims 1 and 3 were objected to for the element recited as "re programmable memory". Claims 1 and 3 have been amended to recite the element as "re-programmable memory". Therefore, Applicants respectfully submit that any grounds for this objection are overcome, and respectfully request acknowledgment thereof.

II. The Obviousness Rejections

Claims 1-3 were rejected under 35 U.S.C. § 103(a) as being unpatentable over various combinations of Gates (U.S. Patent No. 4,969,083) in view of Lin et al. (U.S. Patent No. 6,026,230). These rejections are respectfully traversed.

None of the cited references, either alone or in any combination, establish a *prima facie* case of obviousness. "To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success.

Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." See MPEP § 2143.

Independent claim 1 recites "a single chip micro controller; internal RAM that is internal to said single chip micro controller; and internal re-programmable read only memory that is internal to said single chip micro controller." Independent claim 2 recites "user program and system sequencing and coordination instructions are compiled together into a single executable firmware module of said programmable logic controller within a single chip." Independent claim 3 recites "within a single chip, a program execution device having a re-programmable memory whose function is limited to program execution of a programmable logic controller within said single chip."

Gates allegedly cites a "programmable logic controller [that] generates data, address and control signals." See Abstract. "The data, address and control signals are generated by a ladder diagram created and modified in a separate personal computer, which may be coupled to the programmable logic controller through an ethernet cable." See Abstract. Gated also allegedly cites that "[t]he components necessary to implement PLC 15 . . . comprise input/output scanner 55 and logic scanner 57. Input/output scanner 55 includes a central processing unit (CPU) 61, random access memory (RAM) 63, read only memory (ROM) 65, ethernet ports 67 and 69 and parallel I/O ports 71 and 73." See col. 3, lines 24-32. Gates then allegedly cites that "CPU 61 is a Motorola 68010 or equivalent. RAM 63 is 128k by 16 bit RAM available from a number of sources. ROM 65 is a 32k by16 bit EPROM." See col. 4, lines 47-49.

Gates does not expressly or inherently teach or suggest "internal RAM that is **internal to said single chip micro controller**; and internal re-programmable read only memory that is **internal to said single chip micro controller.**" In addition, Gates does not expressly or inherently teach or suggest that "user program and system sequencing and coordination instructions are compiled together into a single executable firmware module of said programmable logic controller **within a single chip**" or "**within a single chip**, a program

execution device having a re-programmable memory whose function is limited to program execution of a programmable logic controller **within said single chip**."

Lin allegedly cites a "Memory Mapping or Memory Simulation system [that] includes a memory state machine, an evaluation state machine, and their associated logic to control and interface with: (1) the main computing system and its associated memory system, (2) the SRAM memory devices coupled to the FPGA buses in the simulation system, and (3) the FPGA logic devices." See Abstract. Lin also allegedly cites "[i]f the operation is a write, address, control, and data signals are transported from the FPGA logic devices to their respective SRAM memory devices" and "[i]f the operation is a read, address, control, and data signals are transported from the SRAM memory devices to their respective FPGA logic devices." See col. 7, lines 40-45.

Lin does not expressly or inherently teach or suggest "internal RAM that is **internal to said single chip micro controller**; and internal re-programmable read only memory that is **internal to said single chip micro controller**." In addition, Lin does not expressly or inherently teach or suggest that "user program and system sequencing and coordination instructions are compiled together into a single executable firmware module of said programmable logic controller **within a single chip**" or "**within a single chip**, a program execution device having a re-programmable memory whose function is limited to program execution of a programmable logic controller **within said single chip**."

Thus, assuming *arguendo* that Gates and Lin cited are combinable (an assumption with which applicant does not agree, because there is no motivation or suggestion to combine Gates with Lin), the combination still does not expressly or inherently teach or suggest all of the claim limitations, and thus does not establish a *prima facie* case of obviousness. Thus, reconsideration and withdrawal of the rejection is respectfully requested.

CONCLUSION

It is respectfully submitted that, in view of the foregoing amendments and remarks, the application as amended is in clear condition for allowance. Reconsideration, withdrawal of all grounds of rejection, and issuance of a Notice of Allowance are earnestly solicited.

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The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. §1.16 or §1.17 to Deposit Account No. 19-2179. The Examiner is invited to contact the undersigned at 732-321-3113 to discuss any matter regarding this application.

Respectfully submitted,

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Date: 12/3/03

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